3700

Utility Patent Application
Docket No. P-181-3 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
Assaf Zeira et al.

10 047 499

Serial No. To Be Assigned

Filed: October 23, 2001

Entitled: METHOD FOR LOCKING SHARED RESOURCES CONNECTED BY A PCI BUS

Examiner

Art Unit

Date: 8 January 2002

Box DAC
Commissioner for Patents
Washington, D.C. 20231

PETITION UNDER 37 CFR 1.10(e) TO GRANT FILING DATE

Dear Sir:

Applicant attaches herewith true copies of the following documents which were deposited with the US Postal Service Express Mail Post Office to Addressee service on October 23rd, 2001:

1. Form PTO SB-05
2. Fee Transmittal PTO SB/17
3. Form PTO SB-01
4. Form PTO SB-35
5. Utility Patent Application: 24 pages
6. _3__ Sheets Of Drawings
7. Certification Of Express Mailing
8. Return Receipt Card

Applicant's attorney has determined, through diligent monitoring of the USPTO's PAIR system and our Deposit Account information, that there appears to be no record of the USPTO ever having received the above-listed documents relating to the filing of a new non-provisional patent application. Further enquiry has been made with the US Postal Service but has only yielded the information that the package was accepted by the USPS on October 23, 2001 and that there is no further information as to its whereabouts. We are aware of the fact that certain mail from October 21 and 22 has been inadvertently destroyed by the US Postal

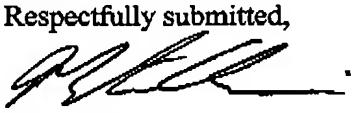
Service in the course of addressing anthrax-cleanup-related issues and we conclude that it is reasonable to assume that mail from October 23rd, including our package, may have suffered a similar fate.

In view of the foregoing, we respectfully petition that the attached application, and accompanying documents, be filed and accorded a serial number and the filing date of October 23, 2001.

In support of the petition, Applicant further attaches herewith a Declaration of Deposit with Express Mail, signed by the employee who deposited the above items as evidenced by the attached true copy of the Express Mail receipt showing the date-in as October 23, 2001, and further corroborated by a screen print taken from a query performed on the US Postal Service Website, confirming the date-in and showing that no further information regarding the package was available as of 12/26/2001 nor when we re-checked on 01/08/2002. Please note that the Express Mailing label number on the query and on the Express Mail receipt are the same as that recorded on the Certificate of Express Mailing which accompanied the items attached herewith, i.e. ET26 5661 462US.

The undersigned further submits herewith authorization to charge our USPTO deposit account the fee required for a petition filed under this section. However, we further request that the fee be waived in view of the extraordinary circumstances.

Respectfully submitted,



Morton Chirnomas
Reg. No. 34,465

Shibolet Yisraeli Roberts & Zisman LLP
350 Fifth Ave., 60th Floor
New York, NY 10118
212-244-4111
212-563-7108 fax

PTO/SB/17 (10-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 130.00

Complete If Known	
Application Number	TO BE ASSIGNED
Filing Date	OCTOBER 23, 2002
First Named Inventor	ASSAF ZEIRA et al.
Examiner Name	
Group Art Unit	
Attorney Docket No.	P-181-3 US

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:
   - Deposit Account Number: 50-1115
   - Deposit Account Name: Shiboleth Yisraeli Roberts & Zisman LLP
   - [X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
   - [X] Applicant claims small entity status. See 37 CFR 1.27
2. [ ] **Payment Enclosed:** [ ] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =	X	=
Independent Claims		- 3** =	X	=
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
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116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
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141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	130
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 130

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	MORTON CHIRNOMAS	Registration No. (Attorney/Agent)	34,465	Telephone	212-244-4111
Signature				Date	01/08/2002

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Utility Patent Application
Docket No. P-181-3 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Assaf Zeira et al. Serial No. To Be Assigned Filed: October 23, 2001 Entitled: METHOD FOR LOCKING SHARED RESOURCES CONNECTED BY A PCI BUS	Examiner Art Unit Date: 8 January 2002 DECLARATION OF DEPOSIT IN EXPRESS MAIL

Box DAC
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, Yvonne James Harris, do hereby declare the following:

1. I am an employee of the law firm of Shiboleth Yisraeli Roberts & Zisman LLP.

2. On October 23, 2001, on the instructions of Morton Chirnomas, I prepared a package bearing Express Mail mailing label **ET 265661462 US** for mailing with the US Postal Service by Express Mail Post Office to Addressee service.

3. Attached are true copies of the documents which I placed in the aforesaid package, listed hereinbelow:

   i. Original Transmittal Letter with Certification of Express Mailing
   ii. Form PTO SB-05
   iii. Fee Transmittal PTO SB/17 for Application
   iv. Form PTO SB-01
   v. Form PTO SB-35
   vi. Utility Patent Application: 24 pages
   vii. _3__ Sheets Of Drawings
   viii. Certification Of Express Mailing
   ix. Return Receipt Card

3. I typed the Express Mail mailing label number **ET 265661462 US** onto the Transmittal Letter and my signature appears on the Certification of Express Mailing, which I dated October 23, 2001, the same date on which I made the deposit directly with an employee of the US Postal Service at their 10118 zip code branch.

4. Attached is a true copy of the Express Mail mailing label receipt showing the date-in as October 23, 2001.

5. Attached are true copies of two printouts, dated 12/26/2001 and 01/08/2002, of the US Postal Service Website showing the answer to our query regarding the delivery status of the package having Express Mail mailing label number **ET 265661462 US** confirming the date of receipt by the USPS as October 23, 2001 and indicating that "[n]o further information is available for this item."

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Yvonne James Harris

Yvonne James Harris

Dated: 1/8/02

Shibolet Yisraeli Roberts & Zisman LLP
350 Fifth Ave., 60th Floor
New York, NY 10118
212-244-4111
212-563-7108 fax

Shipping center *Track & Confirm*

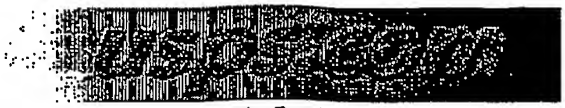
Delivery Status

You entered ET26 5661 462U S

Your item was accepted at 4:14 pm on October 23, 2001 in NEW YORK, NY 10118. No further information is available for this item.

Request Delivery Record >

Enter number from shipping receipt
the field below:



Shipping center
Ship
Rates
Supplies
Web Tools

Track & Confirm
Delivery Confirmation
Signature Confirmation

Keyword/Search

Shipping center Track & Confirm

Delivery Status

You entered ET26 5661 462U S

Your item was accepted at 4:14 pm on October 23, 2001 in NEW YORK, NY 10118. No further information is available for this item.

Request Delivery Record >

Track & Confirm

Enter number from shipping receipt the field below:

POSTAL INSPECTORS
Preserving the Trust

site map | contact us | FAQs | search | keywords

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

"Express Mail" Mailing Label Number ET 265661462 US

I hereby certify that this paper and/or fee, and the items listed below, are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on 23 October 2001 and is addressed "Box PATENT Application, Assistant Commissioner for Patents, Washington, D.C. 20231."

Yvonne James Harris 10/23/01
Yvonne James Harris

Utility Patent Application
Docket No. P-181-3 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Assaf Zeira et al. Serial No. To Be Assigned Filed: Herewith Entitled: METHOD FOR LOCKING SHARED RESOURCES CONNECTED BY A PCI BUS	Examiner Art Unit Date: October 23, 2001

Assistant Commissioner of Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

TRANSMITTAL LETTER AND EXPRESS MAIL CERTIFICATION

Dear Sir:

Enclosed herewith please find the following:

1. Form PTO SB-05
2. Fee Transmittal PTO SB/17
3. Form PTO SB-01
4. Form PTO SB-35
5. Utility Patent Application: 22 pages
6. _3__ Sheets Of Drawings
7. Certification Of Express Mailing
8. Return Receipt Card

Respectfully submitted,

Morton Chirnomas
Reg. No. 34,465

Shibolet Yisraeli Roberts & Zisman LLP
350 Fifth Ave., 60th Floor
New York, NY 10118
212-244-4111
212-563-7108 fax

Inventor: Assaf Zeira, et. al.

Docket No: P-181-3 US

Title: METHOD FOR LOCKING SHARED RESOURCES CONNECTED BY A PCI BUS

The following documents listed below have been received in the United States Patent & Trademark Office on the date stamped hereon:

Form PTO SB-05;
1. Fee Transmittal PTO SB/17;
2. Form PTO SB-01;
3. Form PTO SB-35;
4. Utility Patent Application: 23 pages;
5. Three (3) Sheets of Drawings;
6. Certificate of Express Mailing; and
7. Return Receipt Postcard.

EXPRESS MAIL NO: ET265661462US
STAMP OF USPTO

Assistant Commissioner
of Patents
Box Patent Application
Washington, DC 20231

Morton Chirnomas, Adv.
SHIBOLETH, YISRAELI,
ROBERTS & ZISMAN, L.L.P
Empire State Building
350 Fifth Avenue - Suite 6001
New York, NY 10118-6098

ZDPP

EXPRESS MAIL
UNITED STATES POSTAL SERVICE®

POST OFFICE TO ADDRESSEE

ET265661462US

ORIGIN (POSTAL USE ONLY)			
PO ZIP Code: 10001	Day of Delivery: ☒ Next ☐ Second	Flat Rate Envelope: ☐	
Date In: 10 23 01 (Mo. Day Year)	☒ 12 Noon ☐ 3 PM	Postage: $ 12.45	
Time In: ☐ AM ☒ PM 16 44	Military: ☐ 2nd Day ☐ 3rd Day	Return Receipt Fee	
Weight: lbs. 8 ozs.	Int'l Alpha Country Code	COD Fee	Insurance Fee
No Delivery: ☐ Weekend ☐ Holiday	Acceptance Clerk Initials	Total Postage & Fees: $ 12.45	

SEE REVERSE SIDE FOR SERVICE GUARANTEE AND INSURANCE COVERAGE LIMITS

OCT 23 2001

Customer Copy
Label 11-B August 2000

☐ WAIVER OF SIGNATURE *(Domestic Only)*: Additional merchandise insurance is void if waiver of signature is requested. I wish delivery to be made without obtaining signature of addressee or addressee's agent (if delivery employee judges that article can be left in secure location) and I authorize that delivery employee's signature constitutes valid proof of delivery.

NO DELIVERY ☐ Weekend ☐ Holiday _____ Customer Signature

CUSTOMER USE ONLY

METHOD OF PAYMENT
Express Mail Corporate Acct. No.

Federal Agency Acct. No. or Postal Service Acct. No. Zeira, et. al, P-181

FROM: (PLEASE PRINT) PHONE (212) 244-4111

Morton Chirnomas, Adv.
c/o Shiboleth, Yisraeli, et. al.
350 Fifth Avenue, #6001
New York, NY 10118-6098

TO: (PLEASE PRINT) PHONE ( )

Assistant Commissioner
of Patents
Box Patent Application
Washington, DC 20231

ZIP + 4: 2 0 2 3 1 + _ _ _ _

FOR PICKUP OR TRACKING CALL 1-800-222-1811 www.usps.com

Please type a plus sign (+) inside this box →

PTO/SB/05 (03-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	P-181-3 US
First Inventor	ASSAF ZEIRA
Title	METHOD FOR LOCKING RESOURCES CONNECTED BY A PCI BUS
Express Mail Label No.	ET265661462 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [X] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [*Total Pages* 23]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 3]
5. Oath or Declaration [*Total Pages*]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] Application Data Sheet. See 37 CFR 1.76

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [ ] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [ ] Other: .....

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: ____/____

Prior application information: *Examiner* ____ *Group Art Unit:* ____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 23366 or [ ] *Correspondence address below*

Name	MORTON CHIRNOMAS				
Address	350 FIFTH AVENUE, 60TH FLOOR				
City	NEW YORK CITY	*State*	NEW YORK	*Zip Code*	10118
Country	USA	*Telephone*	212-244-4111	*Fax*	212-563-7108

Name (Print/Type)	MORTON CHIRNOMAS	*Registration No. (Attorney/Agent)*	34,465
Signature		*Date*	10/23/01

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

PTO/SB/17 (10-01)
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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 496

Complete If Known	
Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Assaf Zeira
Examiner Name	
Group Art Unit	
Attorney Docket No.	P-181-3 US

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SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	17	-20** =	0	X	=
Independent Claims	6	- 3** =	3	X 42	= 126
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
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SUBTOTAL (2) ($) 126

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

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169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	MORTON CHIRNOMAS	Registration No. (Attorney/Agent)	34,465	Telephone	212-244-4111
Signature				Date	October 23, 2001

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

PTO/SB/01 (03-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[X] Declaration Submitted with Initial Filing OR [ ] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	P-181-3 US
First Named Inventor	ASSAF ZEIRA
COMPLETE IF KNOWN	
Application Number	TO BE ASSIGNED
Filing Date	HEREWITH
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR LOCKING SHARED RESOURCES CONNECTED BY PCI BUS

(Title of the Invention)

the specification of which

[X] is attached hereto

OR

[ ] was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

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Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION — Utility or Design Patent Application

Direct all correspondence to: [X] Customer Number or Bar Code Label [ ] OR [ ] Correspondence address below

Name: MORTON CHIRNOMAS

Address: SHIBOLETH YISRAELI ROBERTS ZISMAN L.L.P.
350 FIFTH AVENUE, SUITE 6001

City	State	ZIP
NEW YORK	NY	10118

Country	Telephone	Fax
USA	212-244-4111	212-563-7108

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR : [ ] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
ASSAF	ZEIRA

Inventor's Signature: | Date: OCTOBER, 2001

Residence: City	State	Country	Citizenship
SHOHAM		IL	ISRAEL

Mailing Address: 57 EMEK AYALON ST.

City	State	ZIP	Country
SHOHAM		73142	ISRAEL

NAME OF SECOND INVENTOR: [ ] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
RON	GOTSDYNER

Inventor's Signature: | Date: OCTOBER, 2001

Residence: City	State	Country	Citizenship
GIVAT SHMUEL		ISRAEL	ISRAEL

Mailing Address: 4 GUSH ETZION ST.

City	State	ZIP	Country
GIVAT SHMUEL		54030	ISRAEL

[ ] Additional Inventors are being named on the ____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

PTO/SB/35 (11-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE

NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)

First Named Inventor	ASSAF ZEIRA
Title	METHOD FOR LOCKING SHARED RESOURCES CONNECTED BY A PCI BUS
Atty Docket Number	P-181-3 US

I hereby certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

10/23/2001
Date

Signature

MORTON CHIRNOMAS
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Method for Locking Shared Resources Connected by a PCI Bus

Field of the Invention

The present invention relates generally to a method for locking shared resources between multiple computer processors. More particularly, the present invention relates to a method for locking resources shared between computer processors which are connected by a PCI bus.

Background of the Invention

Early computer systems, i.e. those which operate on a single task at a time, and use a single processor in a system, did not require any locking mechanism to prevent one task or processor from being accessed simultaneously by another task or processor. In many modern computer system, multiple processors, and, in some cases, multiple tasks in each processor, attempt to access a shared resource simultaneously. The problem with such simultaneous action is that, due to a certain sequence of events, the content of the resource, or the way it is handled, may be incorrect.

Therefore, processing systems having concurrently operating processors accessing certain shared resources must have a means for synchronizing such accesses. One way of implementing such a system is the busy-waiting strategy, in which each processor makes a request

for a resource and waits idly until the resource is available. When the busy resource does eventually become available, one requesting processor gains access to the resource, while others continue to await an opportunity to access.

A process called "locking" has been widely used in the industry as a means for ensuring data integrity to better control accesses of tasks and processors to shared resources. The basic idea is to lock a resource against use by other tasks or processors, while a certain task or processor is using the resource. As a result of locking, the resource becomes unavailable to all tasks or processors other than the task or processor that initiated the lock. Upon completion of the requested task or tasks by the resource, the task or processor "unlocks" the resource, effectively opening it or making it available for use by other tasks or processors of the system. Multiple approaches of handling such cases have been suggested in prior art, many of which rely on a central controlling unit, or "interest manager", to handle the locking and permission setting for such locking mechanisms.

Many modern computer systems use a bus known as a Peripheral Component Interconnect (PCI) bus. The PCI buses have a locking mechanism, [LOCK#], to guarantee exclusive access to particular system resources whenever a device on the PCI bus requests ownership of the bus, or in other words, to perform an "atomic access", i.e. uninterruptible access, to a resource. When LOCK# is asserted,

nonexclusive transactions must proceed to an address that is not currently locked, or otherwise wait until such lock is deactivated. A grant to start a transaction on the PCI bus does not guarantee control of LOCK#. Moreover, the system requires exclusivity on a region of 16 aligned bytes. The lock mechanism that controls LOCK# must be separately implemented. By assigning a resource a lock status, the mechanism will prevent the access to such locked resource.

Many modern processors provide support for locking mechanisms such as test-and-set, compare-and-swap, or fetch-and-add. Test-and-set(t) atomically (i.e. in a single step) reads the original value of "t" and sets it to "1". Compare-and-swap(a, b) atomically swaps the data values between "a" and "b". Fetch-and-add (x, n) atomically reads the original value of "x" and adds "n" to it.

As the known systems for locking mechanisms are relatively time consuming and complex, there clearly exists a need in the industry for providing a system and method for efficient resource-locking mechanism, specifically for the use in PCI-based or similar systems.

Objects and Summary of the Invention

The present invention relates generally to systems where memory of one central processing unit (CPU) in a multiple processor system may be accessed by another CPU. Furthermore, the present invention is particularly related to a system wherein a resource memory table is used

with memory resources dedicated for each processor and shared resource combination More specifically this invention is related to the case where, in such a multi processing system, the write and read operations of each processor are directed to specific memory elements in the resource memory table; for write operations, each processor is directed to access a single memory element per resource while for read operations each processor is directed to access two or more memory elements simultaneously, per shared resource. A memory element may be a bit, a byte, or otherwise an indivisible basic memory unit.

It should be understood that in the context of this invention, the term "CPU" is being used to include any sort of computational processing unit, including a network processor, a microprocessor, a microcontroller, and the like.

The present invention relates to a method for locking a resource which is shared by a plurality of processors. Each resource has a memory unit related to it and which can be automatically accessed, over PCI bus or by any other communication means having similar memory cycles characteristics, by the processors sharing the resource. Employing the method in a system such as that described results in a fast locking and unlocking mechanism.

A specific example of such a bus is that of the PCI bus. Even more specifically the invention relates to a system comprised of multiple

packet processors in service aware networks (SAN) where wire-speed performance is essential to ensure high quality of network service.

It is a purpose of this invention to provide an improved apparatus and method for efficiently locking resources connected to multiple processors over a PCI bus or over any other communication means having the same or similar memory cycle characteristics. An exemplary embodiment of a computer system embodying the present invention comprises at least two CPUs, shared memory, at least one shared system resource and a resource-locking table provided in the shared memory, wherein each of the CPUs is communicatively interconnected with the shared memory and the shared system resource, and the resource locking table is operative by each of the CPUs.

Brief Description of the Drawings

Fig. 1 is a diagram of an exemplary of a PCI-bus based computer system;

Fig. 2 is a diagram of shared memory which may be used for purposes of locking shared resources in accordance with an exemplary embodiment of the present invention;

Fig. 3 is a flow chart of an exemplary embodiment of the shared resource locking mechanism of the exemplary embodiment; and

Fig. 4 is a diagram of an exemplary embodiment of shared memory used for locking shared system resources in accordance with an exemplary embodiment of the system of the present invention.

Detailed Description of the Invention

With reference to FIG. 1, a system **100** contains multiple processing units CPU1 to CPU N (hereinafter CPUs) **110-1 – 110-n,** where N is 2 or greater (thus at least two CPUs are required). CPUs **110**are connected via PCI bus **140**, or any other communication means having similar memory cycles characteristics, i.e. where the write operation can be atomically performed to a single memory element while a read can access at least two or more elements simultaneously. However, it should be noted that bytes are used herein only for the purpose of example, and any basic memory element can be used. Each CPU **110** has, in addition to its own memory, access to shared memory **130** which is accessible by the other CPUs **110**, and which is also connected to PCI bus **140**. In some embodiments of this invention shared memory 130 may be part of the memory of a CPU. In addition, at least one shared system resource **120** is also connected to PCI bus **140**. At times, one of CPUs **110**, specifically CPU **110-1** for purposes of this example, may wish to request exclusive access to a shared resource, for example, resource **120-1**, i.e. simultaneously prevent any other CPU **110-2 – 110-**

n, to connect with shared resource **120-1**, but without disrupting the possibility of use of other shared resources **120-2 – 120-m**. In accordance with the present invention, each CPU **110**is provided with control commands **150** that allow for the implementation of a locking mechanism that will prevent access of any other CPU **110** to shared resource **120** while it is being exclusively used by CPU **110-1**. The operation of CPUs **110**may be totally independent from one another and CPU **110-1** may use data provided by shared resource **120-1** at a rate that is not under the control of any of the other CPUs.

In an exemplary embodiment of the present invention, where N=4, CPUs **110-1 through 110-4** are connected to PCI bus **140**. A portion of shared memory **130** is assigned for the purpose of use in conjunction with the locking mechanism control commands **150**.

A schematic diagram of shared memory **130** is shown in Fig. 2. The portion of shared memory **130** which is dedicated to locking mechanism control commands **150** is divided into ownership rows **220**; one ownership row for each resource, i.e. row **220-1** is dedicated to the first shared resource, row **220-r** to the r^{th} resource, and row **220-m** to the last shared resource. In the case where four CPUs are used (i.e., n=4), each byte of a four-byte double word, is used as an owner field for a specific CPU **110**. Hence, byte 0 **210-1** corresponds to CPU **110-1**, and byte 1 **210-2** corresponds with CPU **110-2**, and so on. This should be understood as, the column of byte 0 corresponds to CPU **110-1**, the

column of byte 1 to CPU **110-2** and so on. It should be noted that the number of bytes in each row is limited only by the maximum number of bytes that CPUs **110** and bus **140** can handle as an atomic read operation. For example, systems capable of handling 8-bytes, could handle eight CPU **110** using the disclosed invention.

A description for an exemplary embodiment employing a hierarchical approach for systems having more CPUs than can be handled by reading one memory row atomically is disclosed below. A CPU **110** claiming exclusive ownership, or requesting to lock resource **120**, for example, for its sole use, first performs a sequence of actions designed to ensure a successful lock without contention with other CPUs **110**, and at the end of the process relinquishes the lock from resource **120-1**, making it available for use by other CPUs **110**. Moreover, although the example relates to a memory row of 32-bits (4 bytes), the system can be easily modified by one of ordinary skill in the art to be used with memory rows of larger or smaller numbers of bytes, for example, 2 bytes, 8 bytes, 16 bytes, etc. or any number of bytes as long as a read operation can be performed atomically, as explained above.

The flow chart in Fig. 3 describes the sequence of steps, according to an exemplary embodiment of the present invention, for achieving a secure lock of a resource **120** for use by CPU **110** ("c"). In checking step **310**, the ownership row **210** corresponding to resource **120** ("r") to be accessed is checked. If the contents of any of the bytes **210-1 – 210-n** is

anything other than "0" then the requesting CPU **110-c** waits in step **330** before attempting to check ownership row **210-r** for another time. A person skilled in the art could program the wait time to correspond to any number of parameters, including the priority of the request, the number of CPU **110** among all other CPUs **110**, the frequency of request for a lock by CPU **110**, the type of resource **120**, and others. However, if ownership row **220-r** is clear, then the system may proceed to locking step **320** where byte **210-c**, corresponding to CPU **110-c** which is attempting to lock resource **120-r** in ownership row **220-r**, is set to "1". Since CPU **110-c** has a designated byte **210-c** in ownership row **210-r**, there is no possibility of contention or override by another CPU **110**. In recheck step **340** ownership row **220-r** is checked to ensure that only one CPU **110** has locked resource "r". If that is not the case, i.e. if another CPU **110** has simultaneously set ownership in its ownership byte **210** to 1, then control is transferred to conflict clearing step **350** where all the bytes **210-1 – 210-n** corresponding to the requesting CPUs **110**are cleared, followed by a wait period in waiting step **330**. When CPU **110** has reached recheck step **340** and received a "No" answer, then resource **120-r** is considered locked, or otherwise exclusive for the use by CPU **110-c**, in access step **360**. Once CPU **110-c** has completed its use of resource **120-r**, CPU **110-c** relinquishes the lock over resource **120-r**, by clearing byte **210-c in row 220-r**.

In system **100** the locking operation requires four PCI transactions: a) read operation in step **310**; b) write operation in step **320**; c) read operation in step **340**; and d) write operation in step **370** (assuming that a simultaneous conflicting request has not been made, triggering step **350**.

Figure 4 shows an exemplary embodiment in which shared memory **130** is organized for implementation of a hierarchical locking system allowing for up to sixteen CPUs **110**. This embodiment may be required in system **100** where bus **140** is limited to reading atomically a maximum of four aligned bytes, for example. In this example, sixteen CPUs **110** are grouped in groups of four CPUs. A table **470** have rows **460-1** through **460-m**, i.e., one row per resource **120**. Each row **460** contains four bytes **430**, each byte corresponding to a group of four CPUs **110**. Byte **430-1** corresponds to CPU **110-1** through **110-4**, byte **430-2** corresponds to CPUs **110-5** through **110-8**, and so on. A table **450** having rows **420** is further provided. A group **450**, corresponding to a single resource **120** is comprised of four rows **420**. Each row **420** contains four bytes **410**, each such byte **410** corresponding with a single CPU. Hence is CPU **110-1** wishes to access resource **120-1** then the first byte **410-1** of row **420-1** of group **450-1** is set to "1" and correspondingly, the first byte **430-1** of row **460-1** of table **470** is set to "1". Therefore, in order to determine the use of resource **120-1**, it is sufficient to read row **460-1** and if any memory element within row **460-1** is set to "1", then the resource is

identified as being in use and unavailable. This exemplary embodiment can be easily modified by one skilled in the art to fit implementation of 2-byte, 8-byte, 16-byte, or otherwise any other implementation allowing for an atomic read of a single row.

Thus the locking procedure takes place in two steps: a) choosing the CPU group **430** for a particular resource; and b) locking the resource for a specific CPU **110**. Therefore steps 310, 320 and 340 shown in Figure 3 must be repeated twice, once for step a) above and then for step b) above. Similarly, upon release of a resource, first the byte in 410 is reset, followed by the byte in 430. The algorithm presented in Figure 3 can now be easily modified by a person skilled in the art, to accommodate for this change. The hierarchy may continue any depth as may be deemed necessary. Moreover, the examples relate to a memory row of 32-bits, however, the system can be easily modified by one of ordinary skill in the art to be used with memory rows of larger or smaller numbers of bytes, for example, 2 bytes, 8 bytes, 13 bytes, 16 bytes, etc. provided that the write operation can be atomically performed. Additionally, it should be understood that the invention can be configured for a different number of CPUs than that shown in the exemplary embodiment. It should also be noted that it is always possible to use fewer CPUs than the maximum shown in each embodiment.

Further modifications and alterations may also be made to the exemplary embodiments of the invention as described herein by one of

skill in the art without departing from the spirit or scope of the invention as claimed in the appended claims.

I claim:

1. A computer system comprising:

at least two CPUs;

shared memory shared by said CPUs,

at least one shared system resource accessible to said CPUs; and

said shared memory having therein a resource locking table, comprising memory elements, each of said memory elements designated for being written to by only one of said at least two CPUs, and each CPU having a corresponding memory element for each shared system resource to which it has access,

wherein each of said at least two CPUs is communicatively interconnected with said shared memory and said shared system resource, and said resource locking table is operative by each of said CPUs.

2. A computer system according to claim 1, wherein said communicative interconnection is across a communications bus wherein a single read operation is capable of atomically reading at least a collection of said memory elements, said collection comprising at least two memory elements.

3. A computer system according to claim 1, wherein said memory element is a bit.

4. A computer system according to claim 1, wherein said memory element is a byte.

5. A computer system according to claim 1, wherein any of said at least two CPUs can read a first collection of memory elements in a single transaction, said first collection of memory elements corresponding to requests of said CPUs for one of said at least one shared system resources.

6. A computer system according to claim 5, wherein a CPU locks a shared system resource by executing control commands to acccomplish the steps of:
a. checking the content of said first collection of memory elements of said shared memory and if all are not clear waiting for all of them to clear;
b. setting the memory element corresponding to said CPU;
c. checking if more than one of said memory elements of said first collection of memory elements is set, and if true then reset said memory element corresponding to said CPU and waiting for all of said memory elements of said

first collection of memory units to reset and repeat the sequence from step a.;

d. access said shared system resource corresponding to said first collection of memory elements; and

e. reset said memory element, corresponding to said CPU, of said first collection of memory elements corresponding to said at least one shared system resource.

7. A computer system according to claim 5, wherein a second collection of memory elements corresponds to a group of CPUs.

8. A computer system according to claim 7, wherein a CPU locks a shared system resource by executing control commands to acccomplish the steps of:

a. checking the content of said second collection of memory elements and, if not clear, waiting for them to all clear;

b. setting the memory element corresponding to a desired CPU group;

c. checking if more than one of said memory elements of said second collection of memory elements is set, and if true then reset said memory element corresponding to said CPU group and waiting for all of said memory elements of said second collection of memory elements to reset and repeat

the sequence from step a.;

d. checking the content of said first collection of memory elements corresponding to said shared system resource and said CPU group and if not clear, waiting for them to all clear;

e. setting the memory element corresponding to a CPU within said CPU group;

f. checking if more than one of said memory elements of said first collection of memory elements is set, and if true then reset said memory element corresponding to said CPU and waiting for all of said memory elements of said first collection of memory elements to reset and repeat the sequence from step a.;

g. accessing said shared system resource corresponding to said first collection of memory elements;

h. resetting said memory element corresponding to said CPU, of said first collection of memory elements corresponding to said shared system resource; and

i.resetting said memory element, corresponding to said CPU group, of said second collection of memory elements corresponding to said shared system resource.

9. A method for locking a shared system resource for use by a single CPU in a multiprocessor, shared memory system, comprising providing a resource locking table in said shared memory which is operative by any CPU in the system, and by

which any individual CPU can: a) update a memory element corresponding uniquely to the shared system resource and CPU; and b) read all memory elements corresponding to the shared system resources.

10. A method for locking a shared system resource for use by a single CPU the method comprising:

a. checking the content of a collection of memory elements of a resource locking table implemented in shared memory and if not all are clear waiting for all of them to clear;

b. setting the memory element corresponding to the CPU;

c. checking if more then one of said memory elements of said collection of memory elements is set, and if true then reset said memory element corresponding to the CPU and waiting for all of said memory elements of said collection of memory units to reset and repeat the sequence from a;

d. accessing the resource corresponding to said collection of memory elements; and

e. resetting the memory element, corresponding to the CPU, of said collection of memory elements corresponding to said shared system resource.

11. A method according to claim 10, wherein said shared memory is connected to a PCI bus.

12. A method for locking a shared system resource for use by a single CPU having access to a first and second collection of memory elements of shared memory, the method comprising:

a. checking the content of said second collection of memory elements and if not clear, waiting for them to all clear;

b. setting the memory element corresponding to a desired CPU group;

c. checking if more than one of said memory elements of said second collection of memory elements is set, and if true, resetting said memory element corresponding to said CPU group and waiting for all of said memory elements of said second collection of memory elements to reset and repeat the sequence from step a.;

d. checking the content of said first collection of memory elements corresponding to said resource and said CPU group and, if not clear, waiting for them to all clear;

e. setting said memory element corresponding to a CPU within said CPU group;

f. checking if more than one of said memory elements of said first collection of memory elements is set, and if true then resetting said memory element corresponding to said CPU and waiting for all of said memory elements of said first collection of memory elements to reset and repeat the sequence from step a.;

g. accessing the shared system resource corresponding to said first collection of memory elements;

h. Resetting said memory element, corresponding to said CPU, of said first collection of memory elements corresponding to said shared system resource; and

i. Resetting said memory element, corresponding to said CPU group, of said second collection of memory elements corresponding to said shared system resource.

13. A method according to claim12, wherein said shared memory is connected to a PCI bus.

14. A computer program product for locking a shared system resource for use by a single CPU, the computer program product comprising:

computer readable medium having thereon software instructions for enabling a system, containing at least two CPUs and at least one shared system resource, to perform predetermined operations comprising:

a. checking the content of a collection of memory elements of a resource locking table implemented in shared memory and if not all are clear waiting for all of them to clear;

b. setting the memory element corresponding to said CPU;

c. checking if more than one of said memory elements of said collection of memory elements is set, and if true then resetting said

memory element corresponding to said CPU and waiting for all of said memory elements of said collection of memory units to reset and repeat the sequence from step a.;

d. access said shared system resource corresponding to said collection of memory elements; and

e. resetting said memory element, corresponding to said CPU, of said collection of memory elements corresponding to said shared system resource.

15. A computer software program product according to claim 14, wherein said CPUs and said shared memory are connected by a PCI bus.

16. A computer program product for locking a shared system resource for use by a single CPU having access to a first and second collection of memory elements of at least one shared memory, the computer program product comprising:

computer readable medium having thereon software instructions for enabling a system, containing at least two CPUs and at least one shared system resource, to perform predetermined operations comprising:

a. checking the content of said second collection of memory elements and if not clear, waiting for them to all clear;

b. setting the memory element corresponding to a desired CPU group;

c. checking if more than one of said memory elements of said second collection of memory elements is set, and if true then resetting said memory element corresponding to said CPU group and waiting for all of said memory elements of said second collection of memory elements to reset and repeat the sequence from step a.;

d. checking the content of said first collection of memory elements residing in a resource locking table implemented in said shared memory and further corresponding to said shared system resource and CPU group and, if not clear, waiting for them to all clear;

e. setting said memory element corresponding to a CPU within said CPU group;

f. checking if more than one of said memory elements of said first collection of memory elements is set, and if true then reset said memory element corresponding to said CPU and waiting for all of said memory elements of said first collection of memory elements to reset and repeat the sequence from step a.;

g. accessing the shared system resource corresponding to said first collection of memory elements;

h. Resetting the memory element, corresponding to said CPU, of said first collection of memory elements corresponding to said shared system resource; and

i. resetting memory element, corresponding to said CPU group, of

said second collection of memory elements corresponding to said shared system resource.

17. A computer software program product according to claim 16, wherein said CPUs and said shared memory are connected by a PCI bus.

Abstract Of The Disclosure

A computer system according to the present invention comprises at least two CPUs; at least one shared system resource accessible to each of the CPUs; and shared memory shared by the CPUs. The shared memory has therein a resource locking table, comprising memory elements. Each of the memory elements is designated for being written to by only one of the at least two CPUs. Each of the at least two CPUs is communicatively interconnected with the shared memory and the shared system resource, and the resource locking table is operative by each of the CPUs.

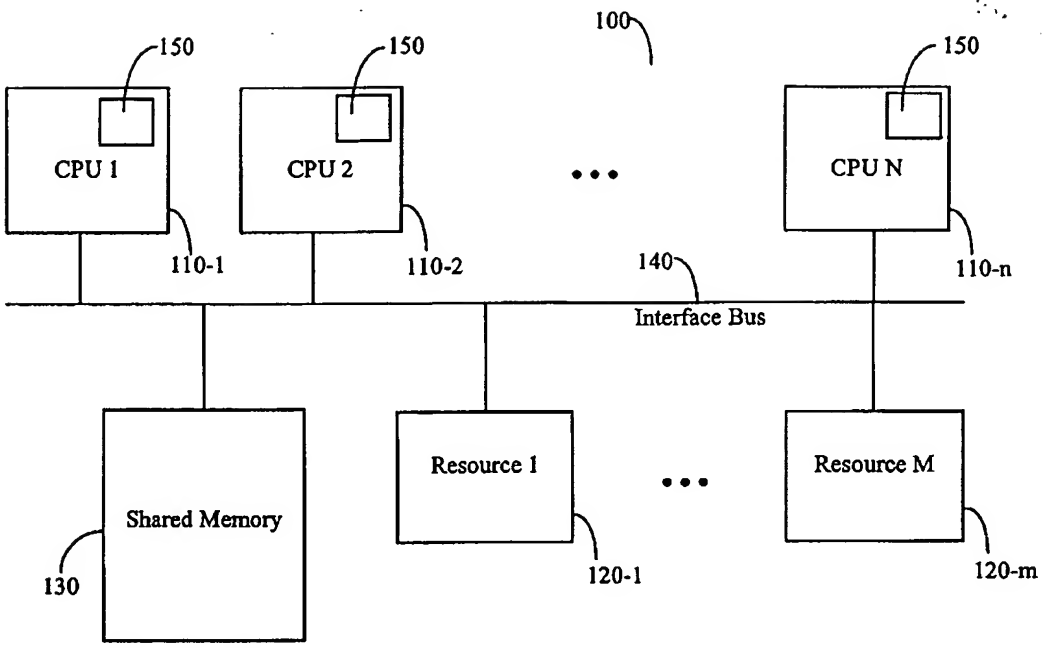
100
150
150
150
CPU 1
CPU 2
CPU N
110-1
110-2
140
110-n
Interface Bus
Shared Memory
Resource 1
Resource M
130
120-1
120-m

FIG. 1

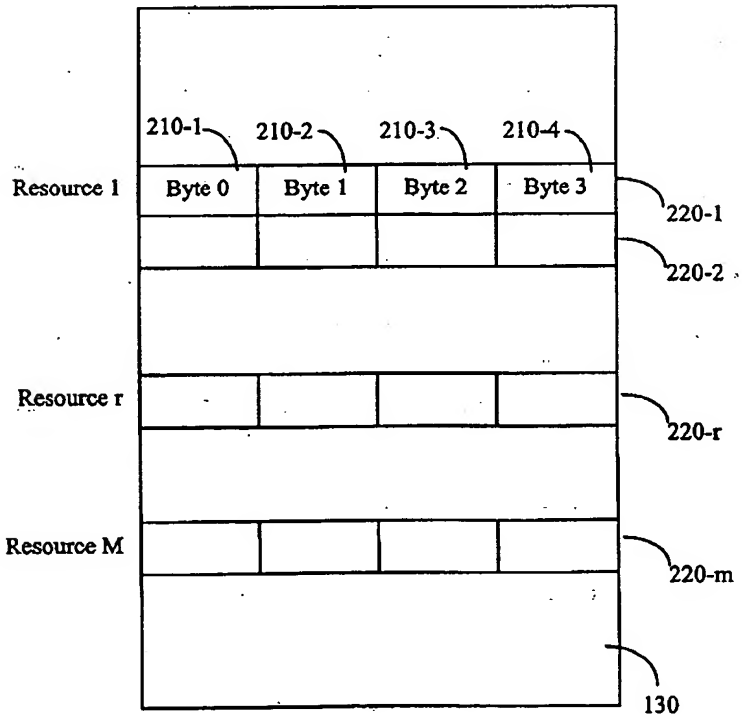
210-1
210-2
210-3
210-4
Resource 1
Byte 0
Byte 1
Byte 2
Byte 3
220-1
220-2
Resource r
220-r
Resource M
220-m
130

FIG. 2

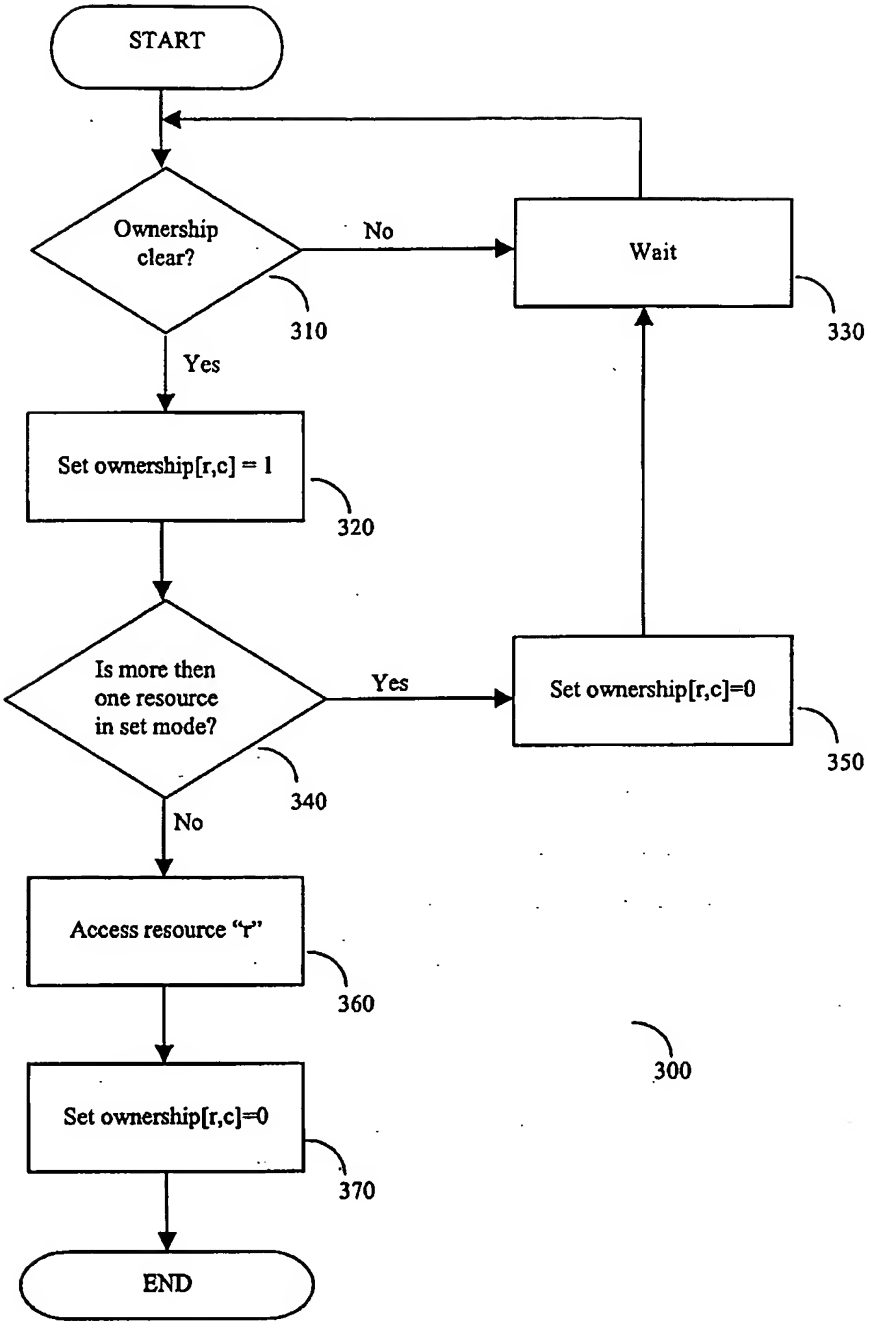
START
Ownership clear?
No
Wait
310
330
Yes
Set ownership[r,c] = 1
320
Is more then one resource in set mode?
Yes
Set ownership[r,c]=0
340
350
No
Access resource "r"
360
300
Set ownership[r,c]=0
370
END

FIG. 3

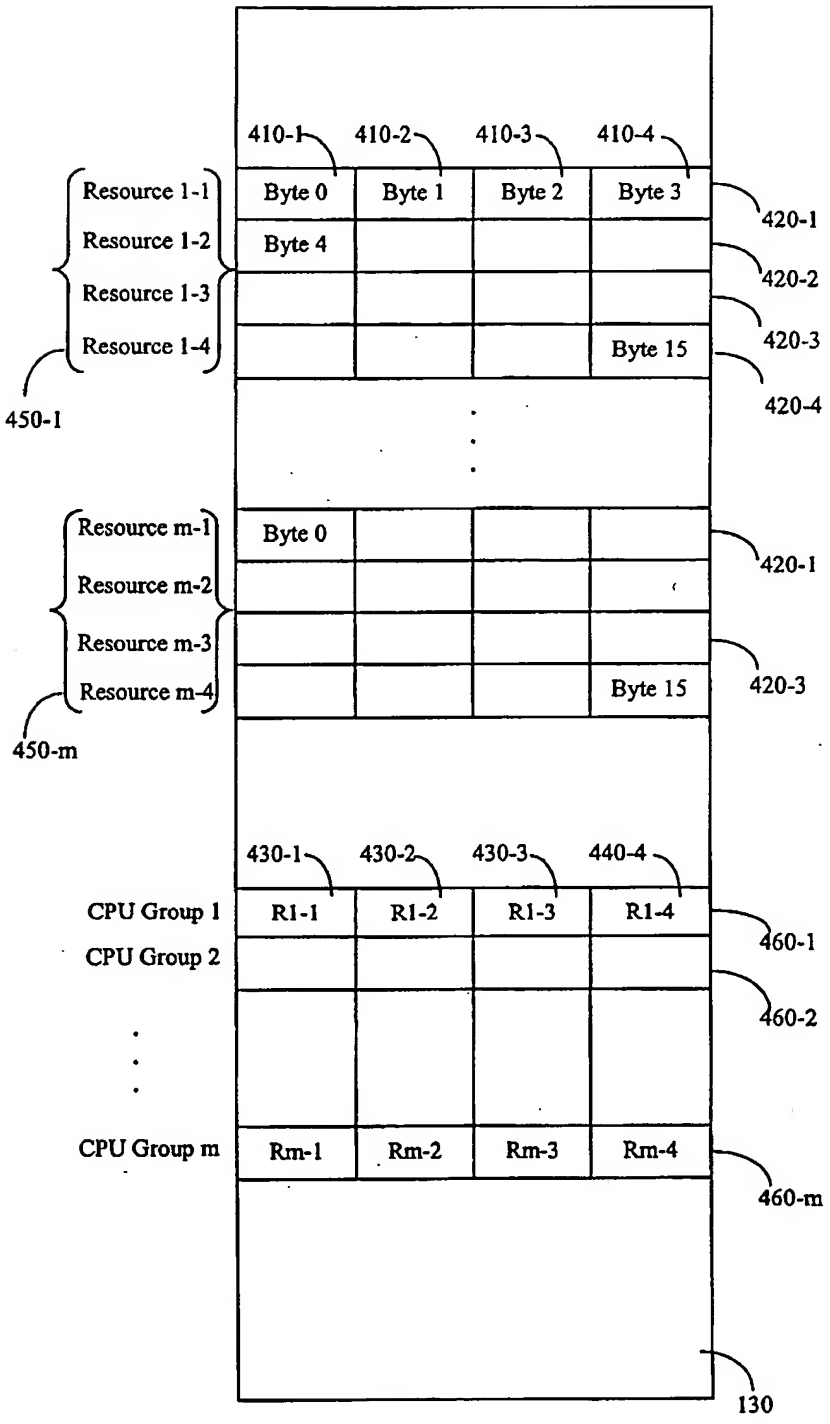
410-1
410-2
410-3
410-4
Resource 1-1
Resource 1-2
Resource 1-3
Resource 1-4
Byte 0
Byte 1
Byte 2
Byte 3
Byte 4
Byte 15
420-1
420-2
420-3
420-4
450-1
Resource m-1
Resource m-2
Resource m-3
Resource m-4
Byte 0
Byte 15
420-1
420-3
450-m
430-1
430-2
430-3
440-4
CPU Group 1
CPU Group 2
CPU Group m
R1-1
R1-2
R1-3
R1-4
Rm-1
Rm-2
Rm-3
Rm-4
460-1
460-2
460-m
130

FIG. 4

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Date: 1/8/02 Yvonne James Harris

Utility Patent Application
Docket No. P-181-3 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Assaf Zeira et al. Serial No. To Be Assigned Filed: October 23, 2001 Entitled: METHOD FOR LOCKING SHARED RESOURCES CONNECTED BY A PCI BUS	Examiner Art Unit Date: 8 January 2002

Box DAC
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Attached for filing please find enclosed:

1. Petition Under 37 CFR 1.10(E) To Grant Filing Date
2. Form PTO SB/17 for Petition
3. Declaration of Deposit with Express Mail
4. Original Transmittal Letter with Certification of Express Mailing
5. Form PTO SB-05
6. Fee Transmittal PTO SB/17 for Application
7. Form PTO SB-01
8. Form PTO SB-35
9. Utility Patent Application: 24 pages
10. _3__ Sheets Of Drawings
11. Certification Of Express Mailing
12. Return Receipt Card

Respectfully submitted,

Morton Chirnomas
Reg. No. 34,465

Shibolet Yisraeli Roberts & Zisman LLP
350 Fifth Ave., 60th Floor
New York, NY 10118
212-244-4111
212-563-7108 fax